Application Note No.M103

CMOS SERIAL E^{2}PROM
TIPS, TRICKS AND TRAPS WHEN USING THE S-29 SERIES AND S-93CxxA SERIES

Contents

Caution This application note describes tips, tricks, and traps to help the design engineer prevent errors and get maximum performance when using S-29 Series and S-93CxxA Series E^2PROMs of Seiko Instruments Inc.
SII manufactures a wide range of E^2PROMs including models that are pin-for-pin compatible with industry standard 93Cxx and 93C(S)xx (same instruction code).

All E^2PROMs (from any manufacturer) may experience a "write" error due to:

- Operation in a low voltage region during power-on / power-off.
- Noise signals causing an error in acknowledging an instruction.

These errors frequently occur when the operating voltage drops below the microcomputer's minimum operating voltage.
Based on the manufacturer's circuit design, certain steps can be taken by the designer to prevent these errors.

1. Tip: Add a resistor to the input pins

All the input pins for the S-29 Series and S-93CxxA Series have a CMOS structure which can produce write errors in a high impedance condition (open pin). Add either a "pull-up" or a "pull-down" resistor per Table 1:

Table 1

Representative E^2PROM model:	S-29130A and S-93C46A	S-29194A
CS pin condition:	Active high (CS)	Active low ($\overline{CS}$)
Resistor:	10 k to 100 kΩ pull-down	10 k to 100 kΩ pull-up

To prevent "write" errors, it is recommended that a pull-up or pull-down resistor be added to the CS pins. For best operation, add the same resistor to the other E^2PROM input pins.

2. Tip: Input /Output pin equivalent circuit.

The input pins have no built-in pull-up or pull-down resistor. The output pin provides a tri-state output (high level, low level, and high impedance). Equivalent circuits are shown in Figure 1 to 4.

2-1. Input pin equivalent circuit

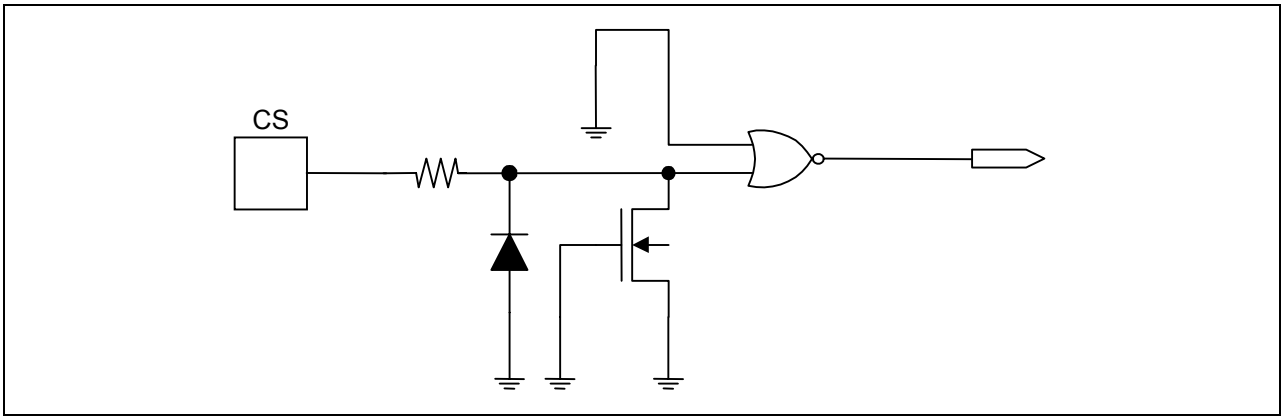


Figure 1 CS pin equivalent circuit

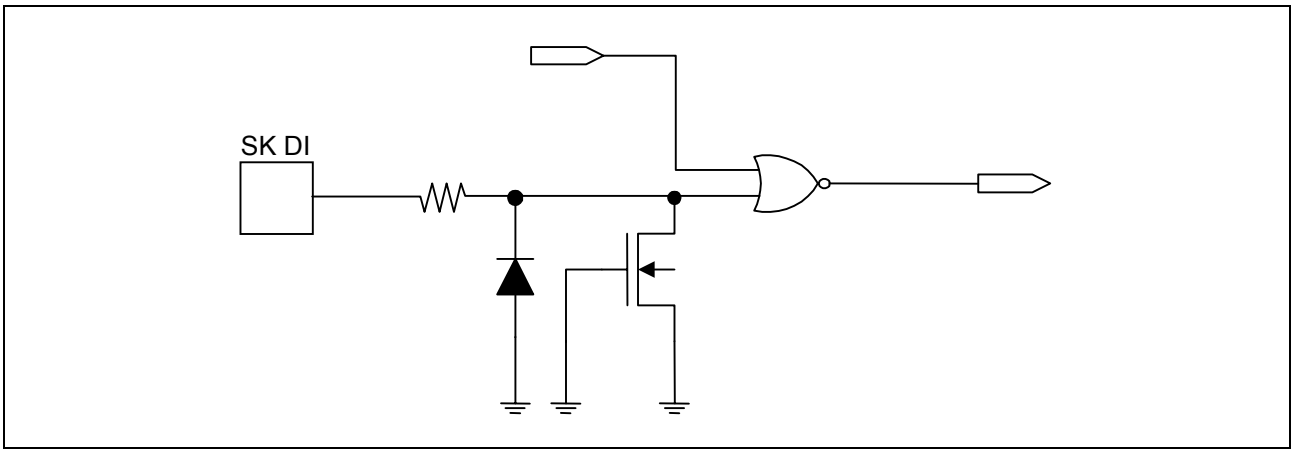


Figure 2 SK DI pin equivalent circuit

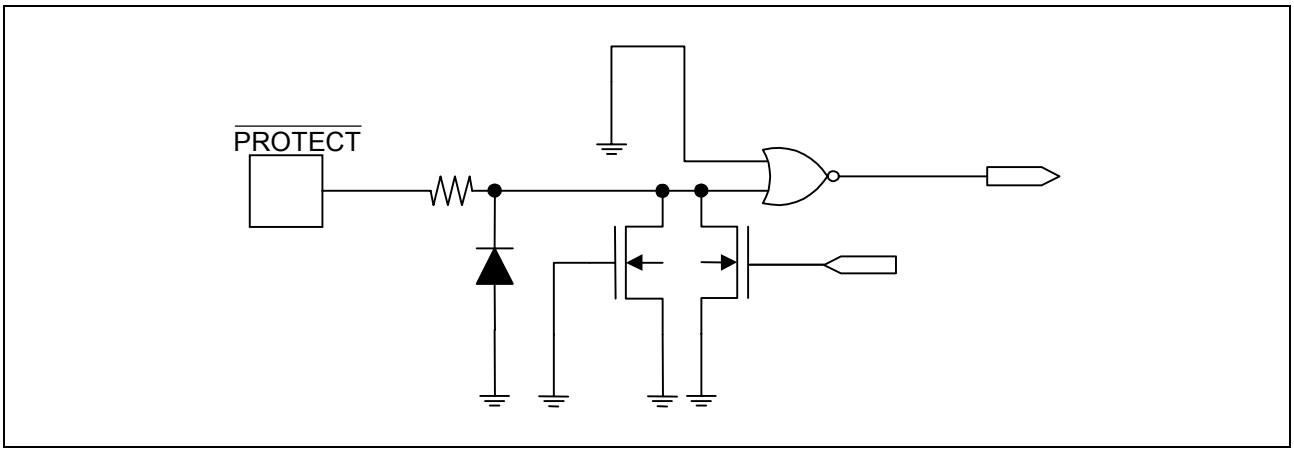


Figure 3 $\overline{\text{PROTECT}}$ pin equivalent circuit

2-2. Output pin equivalent circuit

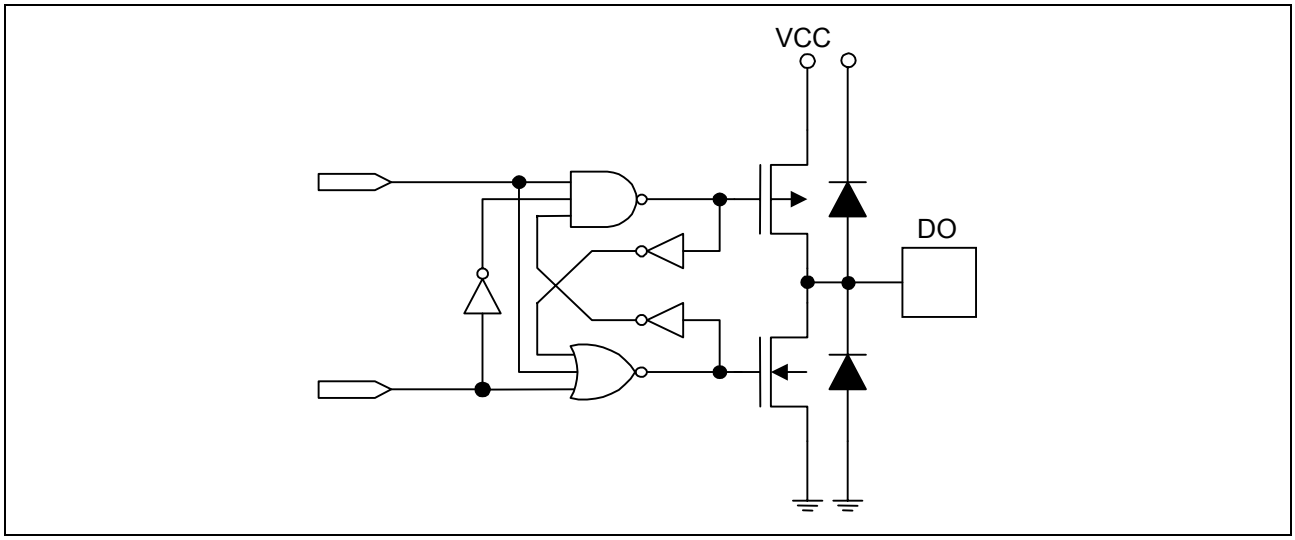


Figure 4. DO pin equivalent circuit

3. Tip: Program disable instruction.

Always execute a “program disable instruction” after the “write” operation has been completed. Once the “program disable instruction” has been executed, the “write” command will not be executed regardless of the instructions.

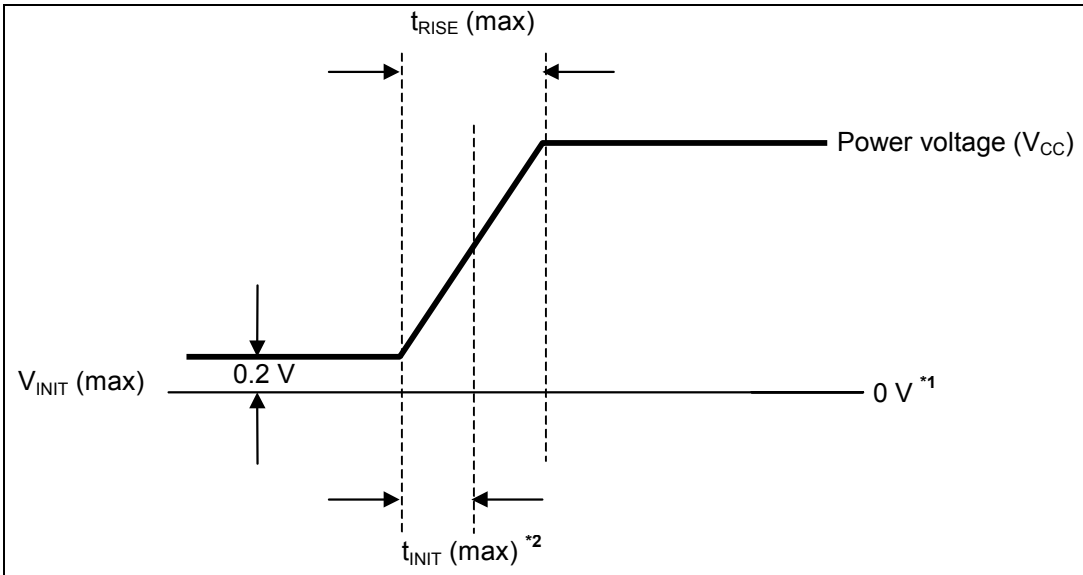
4. Tip: Applying the supply voltage

Seiko Instruments E^{2}PROMs have a built-in “power-on clear” circuit. The power-on clear circuit is one that initializes the IC when the supply voltage is raised, for purposes of avoiding false operations. Follow the procedure below to apply the supply voltage in a safe manner.

4-1. To secure correct operation of power-on clear circuit

Starting at a maximum of 0.2 V as shown in Figure 5, increase the supply voltage to your operating value within the time frame t_{RISE}. *Note that the value of t_{RISE} will change depending on your operating voltage.* (Refer to Figure 6.)

For example:
- If your E^{2}PROM supply voltage = 5.0 V,
- t_{RISE} = 200 ms (from Figure 6),
- increase the V_{CC} to 5.0 V within 200 ms. (Refer to Figure 5.)



***1.** "0 V" means there is no difference in potential between the VCC pin and the GND pin of the E^2PROM
***2.** t_{INIT} is the time required to initialize the E^2PROM. No instructions are accepted during this time.

Figure 5. Increase of the supply voltage

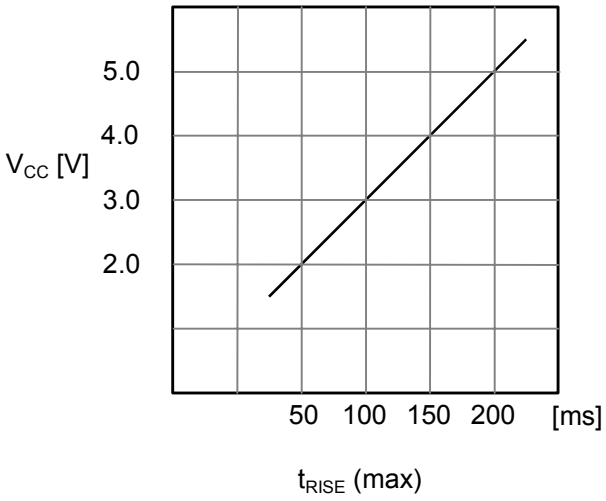


Figure 6. V_{CC} vs. t_{RISE} (max.)

4-2. Trap: Wait for the initialization sequence to complete.

The E²PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relation between initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in Figure 7.

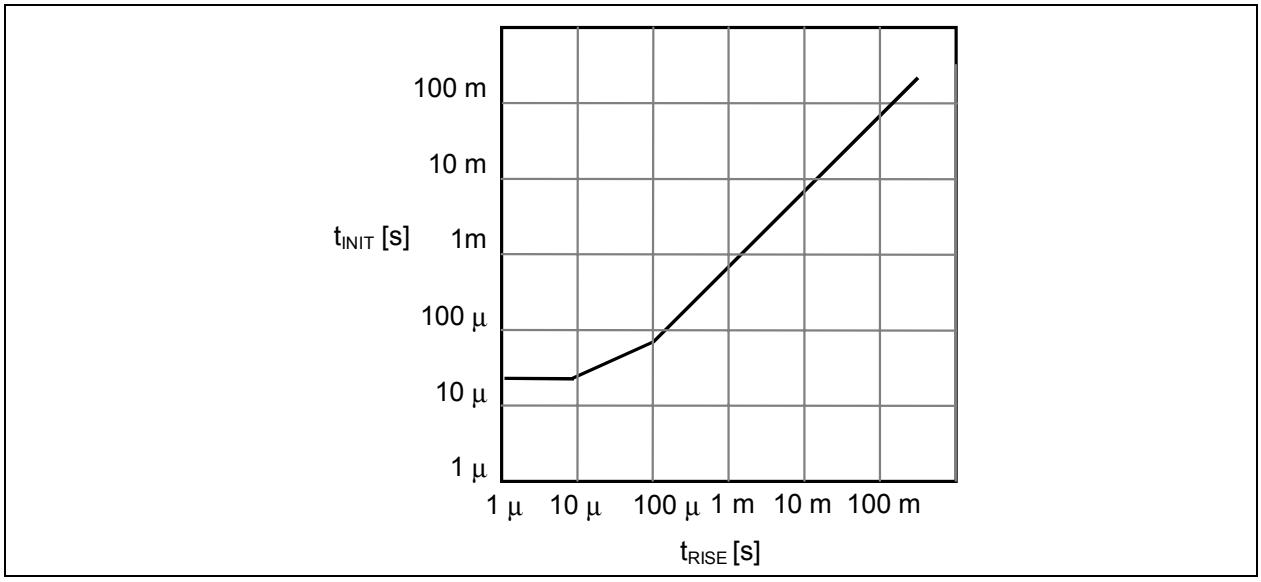


Figure 7 t_{INIT} vs. t_{RISE}

For example, it will take some 20 µs of t_{INIT} when the supply voltage is raised in 10 µs.

4-3. Trap: Problems in the power-on clear circuit.

Once the power-on clear circuit has been used to complete initialization, writing to the E²PROM is disabled (program disable).

If the power-on clear circuit does not operate properly, the following explanation may apply:

- A previous input instruction may still be valid. If, for example, a program enable instruction still remains valid and the E²PROM improperly acknowledges a "write" instruction under the influence of heavy external noise to the input pin during the entry of a next instruction, the E²PROM may unduly execute the "write" instruction.

One of the following causes is suspected in case the power-on clear circuit does not operate:

- Consider the case when the power lines of the microcomputer and the E²PROM are separated from each other, and the output pin of the microcomputer and that of the E²PROM are wired-ORed. In this case, you should check for a difference in potential between the power lines of the microcomputer and the E²PROM. If the microcomputer has a higher voltage, a current from the output pin of the microcomputer tends to reach the power line of the E²PROM, via its DO pin. This will cause the supply voltage of the E²PROM to be held at an intermediate potential, which could disable the power-on clear operation.
- The voltage may have fallen, for example, because the power was turned off during an access to the E²PROM. Even when the microcomputer is reset due to a voltage drop, the E²PROM may produce false operation, if the conditions of power-on clear operation described above for the E²PROM are not met.

5. Trap: Precaution on the data write

Do not lower CS while 16 bits of data are being transmitted. Otherwise, false "write" operation could take place. Figure 8 represents a sample timing of this false "write" operation.

By taking Model 1K-bit S-93C46A as an example, Figure 8 shows the timing with which a "write" instruction is acknowledged and the timing with which a "write" is started, in the case where CS is lowered during the transmission of 16 bits of write data to the E^{2}PROM.

The E^{2}PROM first acknowledges a "write" instruction at the rise of SK with which address A0 is obtained. In Figure 8, this occurs at the rising edge of the 9th clock of SK (the instruction will not be acknowledged, if the number of clocks in Figure 8 is less than 9.)

Upon receiving one bit of data, D15, after acknowledging the "write" instruction as described above, the E^{2}PROM gets ready to start a "write."

Thus, the E^{2}PROM starts a "write" when CS is lowered before the E^{2}PROM has received 16 bits of data, as illustrated in Figure 8.

When the data written in the manner shown in Figure 8 are read out, the value of D15 that was written immediately before this operation is delivered as read-out data D0, due to the internal register of the E^{2}PROM, as can be seen in Figure 9. The other read-out data, D1 to D15, are undefined.

Model S-2900A does not execute a "write" if CS is lowered during the transmission of 8 bits of data.

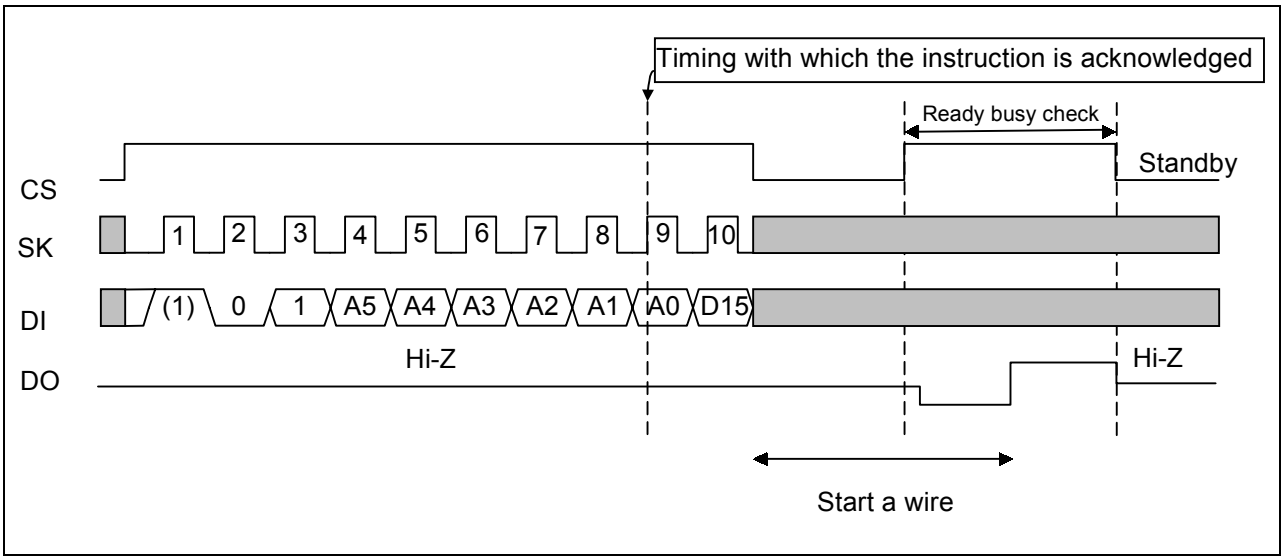


Figure 8 Wrong "write" instruction: when CS is lowered during the transmission of write data.

If the E²PROM executes a "write" after the CPU has sent out D15, as shown in Figure 8, the data in D15 is stored in D0 of the E²PROM register. (Refer to Figure 9.)

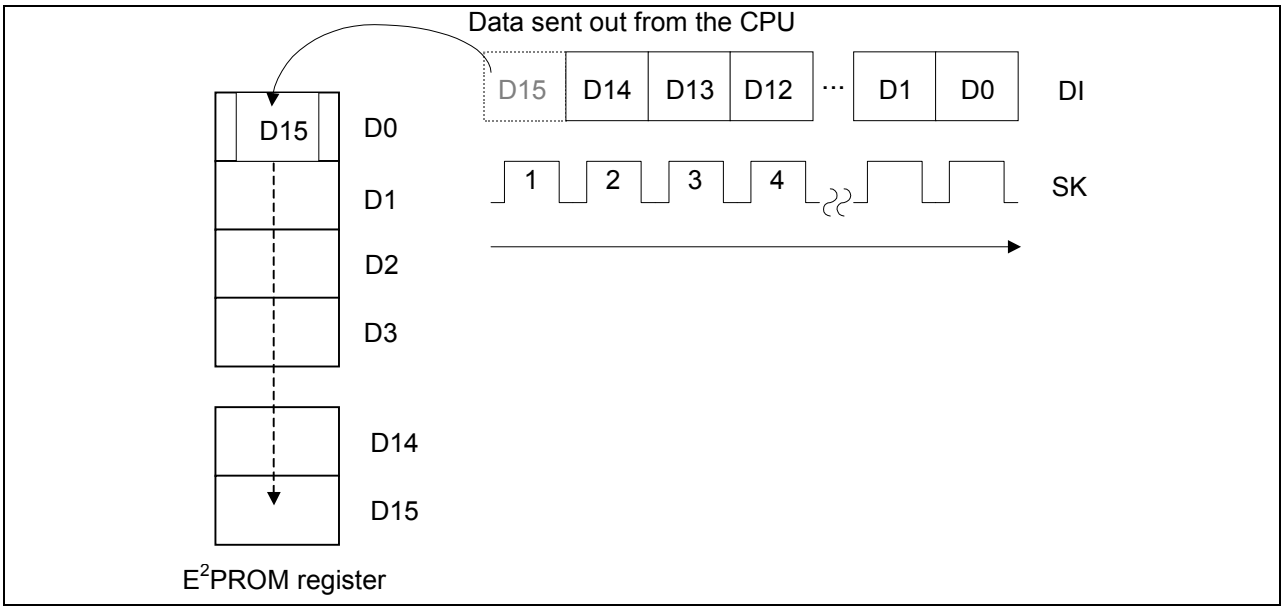


Figure 9 When the data of D15 is stored in register D0 by mistake.

6. Trap: "Write verify operation".

E²PROM does not perform the "Verify" of write data that is usually done by other ordinary memories. The "Write verify operation" is meant to discern whether the E²PROM is in the process of a "write" (Busy) or it has completed a "write" (Ready). (Refer to Figure 10.)

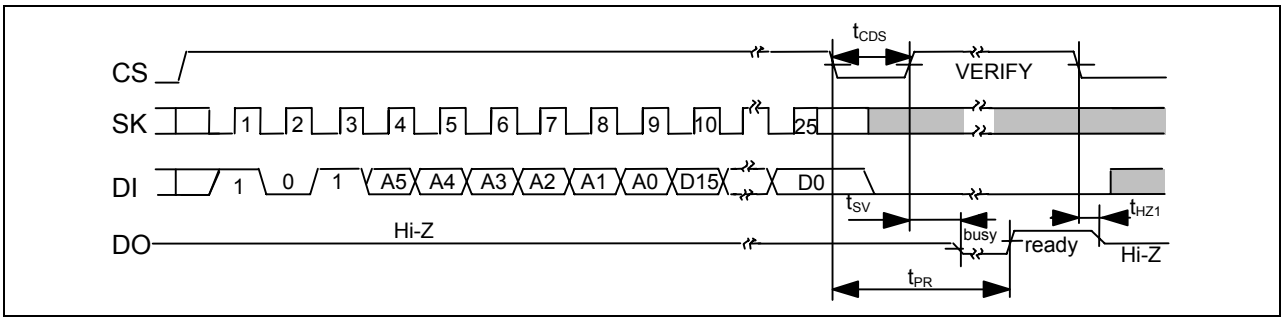


Figure 10 WRITE Timing

7. Trick: Suppressing noise at the input terminals.

The S-29 Series and S-93CxxA Series of E^2PROMs have a built-in low pass filter to suppress noise on the CS, DI, & SK terminals. If the supply voltage is 5.0V, noise with a pulse width $\leq$ 20 ns will be eliminated (at 25°C). (Refer to Figure 11.):

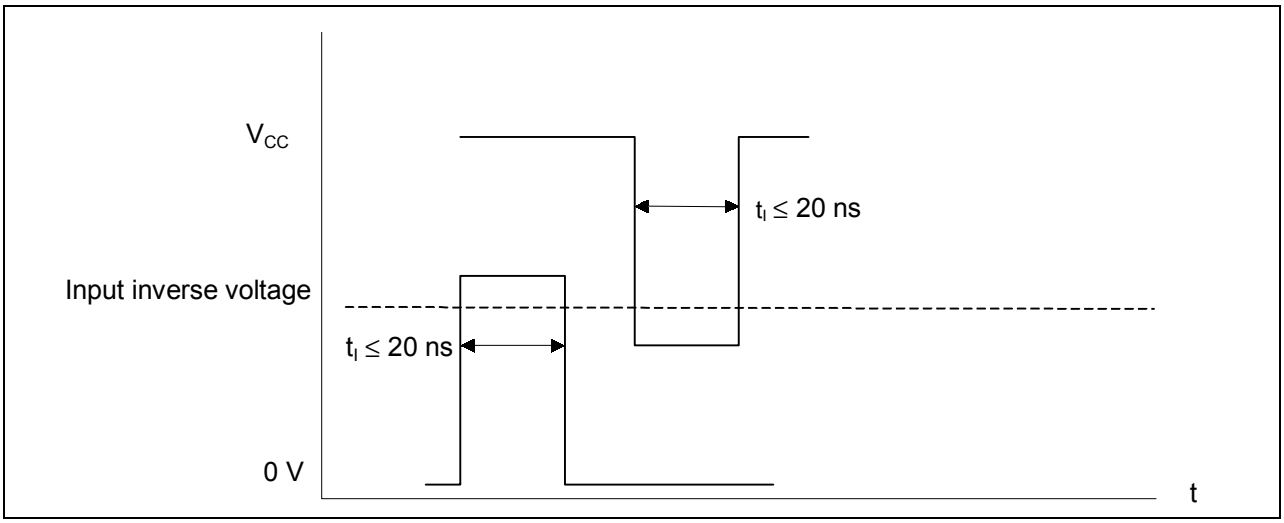


Figure 11 Pulse width (max) that can be eliminated even if the input inverse voltage is exceeded when V_{CC} = 5.0 V

Trap: Noise with a pulse width > 20 ns will be recognized as an input pulse if $V_{CC} > V_{IH}/V_{IL}$.

8. Trap: Severe environments.

Absolute maximum ratings: Do not operate these ICs in excess of the absolute max ratings, as listed on the data sheet. *Exceeding the supply voltage rating can cause latch-up.*